

	Type	Hits	Search Text	DBs	Time Stamp
1	IS&R	529	(257/324,326).CCLS.	USPAT; US-PGPUB	2003/07/08 13:47
2	BRS	57	((257/324,326).CCLS.) and @pd>20021106	USPAT; US-PGPUB	2003/07/08 13:50
3	BRS	38	(trench adj isolation) same (charge adj storage)	USPAT; US-PGPUB	2003/07/08 13:59
4	BRS	410	(trench adj isolation) same (floating adj gate)	USPAT; US-PGPUB	2003/07/08 13:59
5	BRS	404	((trench adj isolation) same (floating adj gate)) not ((trench adj isolation) same (charge adj storage))	USPAT; US-PGPUB	2003/07/08 14:00
6	BRS	9	("5051795"   "5622881"   "5698879"   "5946230"   "6130129"   "6159801"   "6222225"   "6281103"   "6323516").PN.	USPAT	2003/07/08 14:13
7	BRS	9	("5622881"   "5698879"   "5859459"   "5889304"   "5946230"   "6130129"   "6140182"   "6159801"   "6222225").PN.	USPAT	2003/07/08 14:14
8	BRS	5	("5173436"   "5208179"   "5229316"   "5352619"   "5413946").PN.	USPAT	2003/07/08 14:18

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 6228713 B1	14	Self-aligned floating gate for memory application using shallow trench isolation	438/257	257/314; 257/315; 257/316; 257/317; 257/318; 257/319; 257/320; 438/201; 438/211; 438/263; 438/264; 438/266; 438/294; 438/295; 438/296	Pradeep, Yelehanka Ramachandramurthy et al.
2	US 6495853 B1	11	Self-aligned gate semiconductor	257/30	257/314; 257/315; 257/318; 257/321; 257/E29.129	Holbrook, Allison et al.